

### **REMARKS**

This paper responds to the Office Action mailed on October 11, 2006.

Claims 1, 4, 9, 22 and 29 are amended, no claims are canceled, and no claims are added; as a result, claims 1-6 and 8-50 are now pending in this application.

Applicant believes that this Office Action has been incorrectly labeled as a final office action, and requests that the Examiner indicate the correct status of the state of prosecution of this application.

Applicant respectfully disagrees with the comment in the second paragraph of the Response to Amendment starting on page 8 of the outstanding Office Action, where it states that “Perpendicular is a right 90 degree angle, and therefore a tapered wall (such as 88 degrees) does not read on the claim”, and submits that Applicant is entitled to the full scope of equivalents for any allowed claims. The degree of verticality is discussed in the specification at least at page 1, lines 25, 26 and 30; page 2, lines 3, 6 and 11, and the profile straightening at page 7, line 30; page 8, line 7; page 26, lines 13, 15 and 20, where it states that the “profile straightening has achieved a second recess 345 that is significantly less tapered, if at all, than the first recess 344 depicted in FIG. 3B”. Thus, one of ordinary skill in the art would easily understand the taught profile straightening to obtain more vertical, or near vertical sidewalls as discussed in the specification and shown in the figures.

### **Information Disclosure Statement**

Applicant submitted an Applicant submitted an Information Disclosure Statement and a 1449 Form. The Examiner indicates that the documents are classified in unrelated classes and appear to be unrelated. The Applicant has not reviewed these documents and defers to the expertise of the Examiner as it appears that he has reviewed the documents to some extent. However, Applicant respectfully requests that initialed copies of the 1449 Forms be returned to Applicant's Representatives to indicate that the cited references have been considered by the Examiner.

§102 Rejection of the Claims

Claims 46-50 were rejected under 35 U.S.C. § 102(b) for anticipation by Lee et al. (KR Publication 2001-037699). Applicant respectfully traverses this rejection.

The cited reference of Lee discloses a method of increasing the total capacitance without increasing the aspect ratio (see abstract lines 1-2). The method first dry etches the fourth oxide and second nitride layers to expose the storage node contact, then deposits polysilicon (11 in figure 1C and 130 in the abstract figure) and fills the holes with a liquid spin on glass 12 (see lines 11-14 and figure 1C). An etch back process results in a smooth top surface with the horizontal portions of the polysilicon exposed, which is then etched to separate the polysilicon 130 inside the storage node contact holes into separate capacitor plates. The third oxide is wet etched to extend the surface area of the lower capacitor plate after the dry etch. Applicant respectfully disagrees with the Examiner's statement on page 2 of the outstanding Office Action that Lee is "forming a conductive structure 130 in the recess having vertical sidewalls", and notes that item 130 is the polysilicon layer, and that there is no suggestion in the description of the sidewalls being vertical. Applicant suggests that the sidewalls are drawn as vertical for simplicity, and not because the disclosed process results in vertical sidewalls. Applicant submits that the disclosed order of dry and then wet etching in Lee teaches against the recited wet then dry etching of the present application. Applicant further notes that the resulting structure does not extend from the initial substrate (120, 100 as kindly pointed out in the Office Action on page 2) that the recess was formed in.

Applicant respectfully submits that the cited reference does not disclose at least the feature of "*...forming a conductive structure in the recess, wherein the conductive structure has vertical sidewalls, is partially embedded in the recess, and wherein the conductive structure is formed to extend from the first dielectric stack ...*", as recited in independent claim 46, from which claims 47-50 directly depend. The present application discusses the near vertical sidewalls at least at page 1, line 25; page 2, lines 6-11, page 5, line 31; page 7, line 30; page 8, lines 2-7; page 26, line 15 and page 31, line 2. The cited reference of Lee does not suggest vertical sidewalls in the description, and the conductive structure is fully embedded in the substrate in which the recess was etched, and thus does not extend from the dielectric.

The dependent claims are held to be patentable at least as depending from a patentable base claim. In view of the above, Applicant requests that this rejection be reconsidered and withdrawn.

§103 Rejection of the Claims

Claim 1-5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (KR Publication 2001-037699) in view of Choi (U.S. 6,080,594) and O'Brien (U.S. 5,817,182). Applicant respectfully traverses this rejection.

The cited reference of Lee have features discussed above. O'Brien has been discussed in previous responses, and is seen as disclosing removal of etch residues. The cited Choi reference is used in the outstanding Office Action to show that it is known to eliminate spin-on-glass by wet etching first, which is in conflict with the dry etch first process flow of Lee.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of “...wherein the exposed first and second portions of the conductive structure extend vertically above the substrate...”, as recited in independent claims 1 and 4, as amended herein, and from which claims 2-3 and 5 depend. Applicant further notes that these to claims recite “...first wet etching to expose a first portion of the conductive structure... and second non-wet etching to expose a second portion of the conductive structure...”, which is in contrast to the disclosure of the cited references. The cited references do not suggest a method having the conductive structure etched away from the support of the initially surrounding dielectric, nor do they suggest the recited order of etches.

The dependent claims are felt to be patentable at least as depending upon patentable base claims. Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claim 6, 8-21 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. in view of Choi, O'Brien and Kang et al. (U.S. Publication 2004/0175884). Applicant respectfully traverses this rejection.

The cited references of Lee, Choi and O'Brien have been discussed above. The Kang reference has been discussed previously and discloses capacitors with a larger diameter at the bottom than at the middle of the capacitor, and thus Kang's sidewalls are not vertical as recited

in the present claims. Note that Kang's figures show that the side walls 280 of the capacitor are outwardly sloping.

Applicant respectfully submits that one of ordinary skill in the art would understand that the present application's etched wall of recess 144 is more vertical due to the straightening etch shown in figure 1C (see pages 7 and 8). Applicant respectfully submits that Kang has no suggestion about nearly vertical capacitor walls, and thus the combination of Kang with the other cited references would teach against the present method and arrangement.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of "...*wherein the exposed first and second portions of the conductive structure extend vertically above the substrate...*", as recited in independent claims 1 and 9, as amended herein, from which claims 6 and 8, and claims 10-21 respectively depend. The suggested combination of references does not provide proper suggestion for a method having the conductive structure etched away from the support of the initially surrounding dielectric, and thus the dependent claims are patentable over the combination.

In view of the above claim amendments, Applicant requests that this rejection be reconsidered and withdrawn.

Claim 40-45 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. in view of Jost et al. (U.S. 5,966,611) and Sell (U.S. Publication 2004/0147074). Applicant respectfully traverses this rejection.

The cited reference of Lee has been discussed above. Jost has been discussed in prior responses and is used in the outstanding Office Action to show that organic sacrificial layers are known. The cited reference of Sell is used in the outstanding Office Action to show that trench capacitors are known to have aspect ratios.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of "...*stripping amorphous carbon from a conductive structure embedded therein having vertical sidewalls, wherein the conductive structure is coupled to a substrate active area, and wherein the conductive structure includes an aspect ratio from about 6:1 to about 25:1 ...*", as recited in independent claim 40, from which claims 41-45 depend. None of the cited references suggest removing amorphous carbon from a conductive

structure embedded therein, such as the film 138 completely surrounding the container capacitor conductive structure 132 of figure 1F. The cited Jost reference, for example at col. 3, line 45, discloses removing a covering layer and not a layer having an embedded conductive structure as one of ordinary skill in the art would easily understand.

Claim 22-39 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. (U.S. 6,764,947) in view of O'Brien. Applicant respectfully traverses this rejection.

The cited reference of O'Brien has been discussed above and is used to show that rinsing is a known process. The cited reference of Chan is seen as suggesting a method for reducing gate conductor line deformation due to thermal mismatch between the underlying dielectric layer and the polysilicon gate electrode, and between the polysilicon and an overlaying amorphous carbon hard mask due to lattice mismatch. The lattice mismatch may cause delamination of the amorphous hard mask formed above the polysilicon (col. 1, line 35). Chan solves the lattice mismatch by adding a silicon dioxide layer 20 between the polysilicon 18 and the amorphous carbon layer 22 (col. 3, line 16). Applicant respectfully submits that the Examiner has misidentified the trimmed stress relief oxide 26 as a sacrificial second film (see page 7 of the present Office Action), wherein one of ordinary skill would easily understand that this is a photo defined hard mask used to etch the underlying horizontal gate electrode into its final form.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of “...*first etching a sacrificial second film to expose a first vertical portion of a conductive structure* ...”, as recited in independent claims 22 and 29, as amended herein. The cited references disclose and suggest a hard mask and not a sacrificial film and do not expose any vertical section of the conductor.

The dependent claims are held to be patentable at least as depending from base claims shown above to be patentable over the suggested combination of references. Applicant respectfully requests that this rejection be reconsidered and withdrawn.

**CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at (508) 865-8211, or the undersigned attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KEVIN TOREK ET AL.

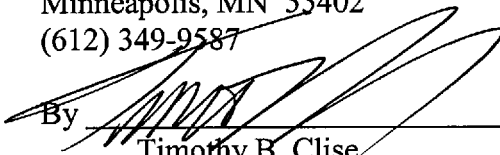
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By



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**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 11 day of December 2006.

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